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EXAMINER	
BELANI, KISHIN G	

ART UNIT	PAPER NUMBER
2143	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/643,331	MCDANIEL ET AL.	
	Examiner	Art Unit	
	Kishin G. Belani	2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/ are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This action is in response to Applicant's amendment filed on 11/27/2007. No claim has been amended. All claims are presented in the original form. **Claims 1-25 are now pending** in the present application. The examiner's prior rejections for **claims 1-25** still stand and are shown below. **This Action is made FINAL.**

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 10, 16-18, 20, 22, and 23 are rejected under 35 U.S.C. 102(e) as being anticipated by **Tillier (U.S. Patent Publication # 6,421,742 B1).**

Consider **claim 1**, Tillier shows and discloses a system for transferring data over a remote direct memory access (RDMA) network (abstract; summary in column 2, lines 21-39 that disclose a system for transferring data over an RDMA network; column 3, lines 34-40 that disclose the same details), comprising:

a host comprising a driver and a network interface card (NIC), the driver being coupled to the NIC (Figs. 1 and 2, I_2O host 101, emulated I_2O I/O unit 103 comprising a device driver 103-2 coupled to an I/O adapter 103-1 (a NIC); column 6, lines 4-14 that describe the same components), wherein the driver and the NIC perform a one-shot initiation process of an RDMA operation (column 3, lines 55-61 that disclose as an example, how in a single message passed from a host, the I/O unit can read and store 1 megabyte of data in an address location of the host memory, without having to interrupt the host CPU multiple times).

Consider **claim 2**, and **as it applies to claim 1 above**, Tillier shows and discloses a system wherein the driver posts a single command message to perform the one-shot initiation process (column 3, lines 55-61 that disclose an example wherein a message passed from a host instructs the I/O unit to read 1 megabyte of data and store it in a specified host memory location).

Consider **claim 3**, and **as it applies to claim 2 above**, Tillier shows and discloses a system wherein the single command message comprises a command to describe pinned-down memory buffers of the host (Fig. 5, map buffer block 506; column 7, lines 40-43 that disclose message parameters "block offset" and "transfer size" of a read or write operation which describe the pinned-down memory buffers of the host).

Consider **claim 4**, and **as it applies to claim 3 above**, Tillier shows and discloses a system wherein the single command message further comprises a command to bind a portion of the pinned-down memory buffers of the host to a steering tag (STag) (Fig. 5, map buffer block 506; column 7, lines 40-43 that disclose message parameters "block offset" and "transfer size" which relate to the address and size of the pinned-down memory buffers of the host; Fig. 8, Pointer (interpreted by the examiner to be a steering tag (STag)) to "Data A" block that addresses Data "A" block, which is a pinned-down memory).

Consider **claim 5**, and **as it applies to claim 4 above**, Tillier shows and discloses a system wherein the single command message further comprises a command to write a send command (Fig. 2, block 201-3 which shows that I_2O remote transport sends a message (created in block 201-2) to I/O unit; flowchart of Fig. 5 that provides details; column 7, lines 24-67 and column 8, line 1 that describe the same details).

Consider **claim 10**, and **as it applies to claim 2 above**, Tillier shows and discloses a system wherein the single command message provides a description of a section of memory (Fig. 1, emulation service block 103-3; Fig. 2, block 201-3 which shows that I_2O remote transport sends a single message (created in block 201-2) to I/O unit; column 6, lines 36-41 which teach that the emulation service 103-3 processes the request for transfer of data by mapping the buffers, and decoding the parameters such

as block offset and length of transfer, thereby disclosing that the message provides a description of a section of memory).

Consider **claim 16**, and **as it applies to claim 1 above**, Tillier shows and discloses a system wherein the NIC comprises an RDMA-enabled NIC (Fig. 2, arrows transferring data between a host 101 and a remote I/O unit 103, that correspond to NICs; column 3, lines 35-40 which disclose that the transferee device has remote direct memory access for target-managed data transfer; column 4, lines 59-66 which disclose that the write command from one host to a remote host is subsequently written to a network interface, thereby disclosing a NIC).

Consider **claim 17**, Tillier shows and discloses a system for transferring data over a remote direct memory access (RDMA) network, comprising:
a host comprising a driver and a network interface card (NIC), the driver being coupled to the NIC (Figs. 1 and 2, I_2O host 101, emulated I_2O I/O unit 103 comprising a device driver 103-2 coupled to an I/O adapter 103-1 (a NIC); column 6, lines 4-14 that describe the same components), wherein the driver and the NIC perform a one-shot completion process of an RDMA operation (Fig. 2, completion message blocks 203-4, 201-5, and 201-6; column 3, lines 55-61 that disclose as an example, how in a single message passed from a host, the I/O unit can read and store 1 megabyte of data in an address

location of the host memory, without having to interrupt the host CPU multiple times; column 6, lines 51-59 that describe the same details).

Consider **claim 18**, and **as it applies to claim 17 above**, Tillier shows and discloses a system wherein the NIC receives a message comprising an optional field carrying a STag value, the STag value being associated with pinned memory in a remote host (Fig. 8, arrow marked 'Pointer to "A"' which the examiner has interpreted to be equivalent to a STag value, being received by NIC along with the "Store Data" command, the pointer value representing the address of the pinned down memory in a remote host).

Consider **claim 20**, and **as it applies to claim 18 above**, Tillier shows and discloses a system wherein the NIC de-associates the STag value with the pinned memory in the host, thereby preventing further access to the pinned memory using the de-associated STag value (Fig. 6, blocks 604-606 that depict freeing up of allocated resources, corresponding to de-associating the STag value from the pinned-memory in the host, thereby preventing further access to the pinned memory using the de-associated STag value; column 8, lines 9-15 that disclose the same details).

Consider **claim 22**, and **as it applies to claim 18 above**, Tillier shows and discloses a system wherein the NIC de-associates the STag value with previously associated SGL information (Fig. 6, blocks 604-606 that depict freeing up of allocated

resources, corresponding to de-associating the STag value pointing to the SGL; cleanup routine of Fig. 7B; column 8, lines 9-15 that disclose the same details).

Consider **claim 23**, and **as it applies to claim 20 above**, Tillier shows and discloses a system wherein the NIC frees any resources dedicated to information regarding the pinned memory (Fig. 6, blocks 604-606 that depict freeing up of allocated resources; cleanup routine of Fig. 7B; column 8, lines 9-15 that disclose NIC freeing up the allocated resources).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness
or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 6-9, 11-15, 19, 24, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Tillier (U.S. Patent Publication # 6,421,742 B1)** in view of **Roach et al. (U.S. Patent Publication # 6,304,910 B1).**

Consider **claim 6**, and **as it applies to claim 4 above**, Tillier discloses the claimed system, except wherein the NIC places the STag value in an optional field in a direct data placement DDP or RDMA header.

In the same field of endeavor, Roach et al. show and disclose a system wherein the NIC places the STag value in an optional field in a direct data placement DDP or RDMA header (Fig. 8 that shows the bit-level definition of each of the two 32-bit word entry shown in Fig. 9; column 8, lines 32-67 and column 9, lines 1-18 that disclose the details of the bit-level structure including BSWA buffer pointer list entries corresponding to the STag values and BLM flag fields indicating validity of the BSWA entries).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the STag value in an optional field in a direct data placement DDP or RDMA header, as taught by Roach et al. in the system of Tillier, so as to be able to handle non-contiguous data blocks during the transfer.

Consider **claim 7**, and **as it applies to claim 6 above**, Tillier discloses the claimed system, except wherein the NIC encodes a value into a field in the DDP or RDMA header indicating that the STag value in the optional field is valid.

In the same field of endeavor, Roach et al. show and disclose a system wherein the NIC encodes a value into a field in the DDP or RDMA header indicating that the STag value in the optional field is valid (Fig. 8 that shows the bit-level definition of each of the two 32-bit word entry shown in Fig. 9; column 8, lines 32-67 and column 9, lines 1-18 that disclose the details of the bit-level structure including BSWA buffer pointer list entries corresponding to the STag values and BLM flag fields indicating validity of the BSWA entries).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to encode a value into a field in the DDP or RDMA header indicating that the STag value in the optional field is valid, as taught by Roach et al. in the system of Tillier, so as to be able to distinguish valid data block entries for remote transfer.

Consider **claim 8**, and **as it applies to claim 6 above**, Tillier discloses the claimed system, except wherein the NIC sets one or more bits in a field in the DDP or RDMA header indicating that the STag value in the optional field is valid.

In the same field of endeavor, Roach et al. show and disclose a system wherein the NIC sets one or more bits in a field in the DDP or RDMA header indicating that the STag value in the optional field is valid (Fig. 8 that shows the bit-level definition of each of the two 32-bit word entry shown in Fig. 9; column 8, lines 32-67 and column 9, lines 1-18 that disclose the details of the bit-level structure including BSWA buffer pointer list entries corresponding to the STag values and BLM flag fields indicating validity of the BSWA entries).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to set a value into a field in the DDP or RDMA header indicating that the STag value in the optional field is valid, as taught by Roach et al. in the system of Tillier, so as to be able to distinguish valid data block entries for remote transfer.

Consider **claim 9**, and **as it applies to claim 6 above**, Tillier discloses the claimed system, except wherein the NIC sets one or more bits or encodes a value into a second field in the DDP or RDMA header to advertise the portion of the pinned memory buffers of the host associated with the STag.

In the same field of endeavor, Roach et al. show and disclose a system wherein the NIC sets one or more bits or encodes a value into a second field in the DDP or

RDMA header to advertise the portion of the pinned memory buffers of the host associated with the STag (Fig. 8 that shows the bit-level definition of each of the two 32-bit word entry shown in Fig. 9; column 8, lines 32-67 and column 9, lines 1-18 that disclose the details of the bit-level structure including BSWA buffer pointer list entries corresponding to the STag values and BLM flag fields indicating validity of the BSWA entries, thereby advertising the portion of the pinned memory buffers of the host associated with the STag).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to set one or more bits or encode a value into a second field in the DDP or RDMA header to advertise the portion of the pinned memory buffers of the host associated with the STag, as taught by Roach et al. in the system of Tillier, so as to be able to distinguish valid data block entries for remote transfer.

Consider **claim 11**, and **as it applies to claim 2 above**, Tillier discloses the claimed system, except wherein the single command message is posted to a command ring of the host.

In the same field of endeavor, Roach et al., disclose a system wherein the single command message is posted to a command ring of the host (Fig. 5A, block 32; column 6, lines 48-64 that disclose a command ring structure as a circular queue of command entries).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to post the single command message to a command

ring of the host, as taught by Roach et al. in the system of Tillier, so as to be able to execute the commands in the FIFO order with opportunity for the non-serviced commands to get multiple turns at the service.

Consider **claim 12**, and **as it applies to claim 11 above**, Tillier as modified by Roach et al., furthermore discloses the claimed system, including wherein the driver allocates an STag value (Fig. 8, arrow marked 'Pointer to "A"' which the examiner has interpreted to be equivalent to a STag value, being allocated by the Input/output unit (combined driver and NIC) and received by NIC, the pointer value representing the address of the pinned down memory in a remote host).

Consider **claim 13**, and **as it applies to claim 12 above**, Tillier discloses the claimed system, except wherein the STag value is returned synchronously from a command call.

In the same field of endeavor, Roach et al., disclose a system wherein the STag value is returned synchronously from a command call (column 6, lines 56-64 which disclose that the host driver increments the "put" pointer whenever a command is queued to the command ring, making the updated pointer (STag value) synchronously available from a call command).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to make the STag value available synchronously from

a command call, as taught by Roach et al., in the system of Tillier, so as to be able to process the transfer of data without any delay.

Consider **claim 14**, and **as it applies to claim 12 above**, Tillier discloses the claimed system, except wherein the STag value is saved in a driver command table of the host.

In the same field of endeavor, Roach et al., disclose a system wherein the STag value is saved in a driver command table of the host (Fig. 3, host memory block 42 and transfer ready queue 60; column 5, lines 44-52 that disclose a lookup field (STag value) inside each frame header includes a pointer to an associated context, and the host driver saves these fields in the host memory 42).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to save the STag value in a driver command table of the host, as taught by Roach et al., in the system of Tillier, so as to be able to process non-contiguous data blocks during the transfer, by using the commands set up in the driver command table.

Consider **claim 15**, and **as it applies to claim 14 above**, Tillier discloses the claimed system, except wherein the STag value saved in a driver command table is associated with an application reference number.

In the same field of endeavor, Roach et al., disclose a system wherein the STag value saved in a driver command table is associated with an application reference

number (Figs. 5A and 5B; column 5, lines 47-52 which disclose that the context field associated with a pointer field (STag value) saved in a driver command table is associated with a small computer systems interface (SCSI) state information interpreted by the examiner to be associated with the application reference number).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to associate the saved STag value in a driver command table of the host with an application reference number, as taught by Roach et al., in the system of Tillier, so as to be able to determine the application that is associated with the transfer of data.

Consider **claim 19**, and **as it applies to claim 18 above**, Tillier discloses the claimed system, except wherein a header of the message indicates the validity of the optional field with a bit flag or specified value in an encoded field.

In the same field of endeavor, Roach et al. show and disclose a system wherein a header of the message indicates the validity of the optional field with a bit flag or specified value in an encoded field (Fig. 8 that shows the bit-level definition of each of the two 32-bit word entry shown in Fig. 9; column 8, lines 32-67 and column 9, lines 1-18 that disclose the details of the bit-level structure including BSWA buffer pointer list entries corresponding to the STag values and BLM flag fields indicating validity of the BSWA entries, thereby indicating the validity of the optional field with a bit flag or specified value in an encoded field).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to indicate the validity of the optional field with a bit flag or specified value in an encoded field, as taught by Roach et al., in the system of Tillier, so as to be able to distinguish valid data block entries for remote transfer.

Consider **claim 24**, Tillier shows and discloses a method for transferring data over an RDMA network (abstract; summary in column 2, lines 21-39 that disclose a method for transferring data over an RDMA network; column 3, lines 34-40 that disclose the same details), comprising:

initiating an RDMA write operation using a one-shot initiation process between a driver and a NIC (column 3, lines 55-61 that disclose as an example, how in a single message passed from a host, the I/O unit (that includes a driver and a NIC) can write and store 1 megabyte of data in an address location of the host memory, without having to interrupt the host CPU multiple times).

However, Tillier, does not show and disclose inserting an STag value in a first field of a DDP or RDMA header of an RDMA send message; and validating the STag value in the first field with a bit flag or other specified value in a second field of the DDP or RDMA header.

In the same field of endeavor, Roach et al. show and disclose inserting an STag value in a first field of a DDP or RDMA header of an RDMA send message (Fig. 8 that shows the bit-level definition of each of the two 32-bit word entry shown in Fig. 9; column 8, lines 32-67 and column 9, lines 1-18 that disclose the details of the bit-level

structure including BSWA buffer pointer list entries corresponding to the STag values); and validating the STag value in the first field with a bit flag or other specified value in a second field of the DDP or RDMA header (Fig. 8 that shows the bit-level definition of each of the two 32-bit word entry shown in Fig. 9; column 8, lines 32-67 and column 9, lines 1-18 that disclose the details of the bit-level structure including BLM flag fields indicating validity of the BSWA entries).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to place the STag value in an optional field in a direct data placement DDP or RDMA header, and set one or more bits or encode a value into a second field in the DDP or RDMA header, as taught by Roach et al. in the method of Tillier, so as to be able to handle non-contiguous data blocks during the transfer and distinguish valid data block entries for remote transfer.

Consider **claim 25**, Tillier shows and discloses a method for transferring data over an RDMA network (abstract; summary in column 2, lines 21-39 that disclose a method for transferring data over an RDMA network; column 3, lines 34-40 that disclose the same details), comprising:

completing an RDMA write operation using a one-shot completion process between a NIC and a driver of a host; and receiving a completion message (Fig. 2, completion message blocks 203-4, 201-5, and 201-6; column 3, lines 55-61 that disclose as an example, how in a single message passed from a host, the I/O unit can write and store 1 megabyte of data in an address location of the host memory, without having to

interrupt the host CPU multiple times; column 6, lines 51-59 that describe the same details).

However, Tillier, does not show and disclose identifying a STag value in a first field of a header of the completion message; and validating the STag value in the first field of the header by identifying a bit flag or other specified value in a second field of the header.

In the same field of endeavor, Roach et al. show and disclose identifying a STag value in a first field of a header of the completion message (Fig. 8 that shows the bit-level definition of each of the two 32-bit word entry shown in Fig. 9; column 8, lines 32-67 and column 9, lines 1-18 that disclose the details of the bit-level structure including BSWA buffer pointer list entries corresponding to the STag values); and validating the STag value in the first field of the header by identifying a bit flag or other specified value in a second field of the header (Fig. 8 that shows the bit-level definition of each of the two 32-bit word entry shown in Fig. 9; column 8, lines 32-67 and column 9, lines 1-18 that disclose the details of the bit-level structure including BLM flag fields indicating validity of the BSWA entries).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to identify a STag value in a first field of a header of the completion message, and validate the STag value in the first field of the header by identifying a bit flag or other specified value in a second field of the header, as taught by Roach et al. in the method of Tillier, so as to be able to handle non-contiguous data blocks during the transfer and distinguish valid data block entries for remote transfer.

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Tillier (U.S. Patent Publication # 6,421,742 B1)** in view of **Futral et al. (U.S. Patent Publication # 5,991,797).**

Consider **claim 21**, and **as it applies to claim 18 above**, Tillier discloses the claimed system, except wherein the NIC delivers the message to the driver, and wherein the driver compares the STag value received with a STag value previously sent.

In the same field of endeavor, Futral et al. show and disclose a system wherein the NIC delivers the message to the driver, and wherein the driver compares the STag value received with a STag value previously sent (Fig. 4, SGL word 2 (chain pointer) that provides address to additional transaction detail element list, when the buffers are scattered across multiple locations, therefore requiring an appended list. In such cases, the driver compares the SGL address received with a prior value to ensure that the same list is being processed with additional buffer addresses in the appended chain list; column 6, lines 36-46 disclose the same details).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide capability in the driver to compare the STag value received with a STag value previously sent, as taught by Futral et al. in the system of Tillier, so as to be able to handle multiple non-contiguous data blocks during the transfer.

Response to Arguments

Applicants' arguments filed 11/27/2007 have been fully considered but they are not persuasive.

The examiner respectfully disagrees with applicants' arguments as the applied references provide adequate support and clarification for claims rejection. Therefore the examiner's rejection of 06/27/2007 is maintained.

Consider **independent claims 1 and 17.** The examiner disagrees with the applicants' argument that Tillier reference fails to disclose "the driver and the NIC [of a host] perform a one-shot initiation [or completion] process of an RMDA operation". The Remote Transport Layer 101-4 of Host 101 in Fig. 1 provides the functionality of a host software driver; a Network Interface Controller (NIC, not shown in Fig. 1, but disclosed in column 1, lines 30-37) teaches the function of a NIC; column 3, lines 35-40 disclose the use of RDMA to transfer data between a host and I/O device; column 3, lines 43-51 disclose a one-shot (using a single command initiation, then without subsequent host interruptions until the transfer is completed) initiation [or completion] process of an RDMA operation. Thus, Tillier reference teaches every feature listed in the applicants' argument, and therefore **rejection for claims 1 and 17** as well as their **dependent claims 2-16 and 18-23** is maintained.

The arguments for the remaining **claims 24 and 25** have already been answered in claims 1 and 17. Therefore, **claims 24 and 25 also remain rejected**.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any response to this Office Action should be **faxed to** (571) 273-8300 **or mailed to**:

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Art Unit: 2143

Hand-delivered responses should be brought to

Customer Service Window
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Kishin G. Belani whose telephone number is (571) 270-

1768. The Examiner can normally be reached on Monday-Thursday from 6:30 am to 5:00 pm.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) or 703-305-3028.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist/customer service whose telephone number is (571) 272-0800.

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